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Design of a MOS-based Transimpedance Amplifier with 3.49kΩ gain and 2.96GHz bandwidth for a Transceiver-level receiver application

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***Abstract* -- This paper describes the design of a transimpedance amplifier, implemented using 0.13µ CMOS technology, with a minimum transimpedance gain of 3k-ohms, a bandwidth of 2.8 GHz and a maximum group-delay variation of 40ps, sustainable to a temperature variation of -40C to 125C and a ±10% fluctuation in the supply voltage. The purpose of this Transimpedance amplifier is to be used as a receiver of SONET/SDH OC-48/STM-16 transceiver to transmit and receive serial data over long-haul (>100km) fiber optics networks at bit rates of up to 2.488 Gb/s.**

Keywords: TIA (Transimpedance Amplifier), shunt-shunt configuration, transimpedance-gain, bandwidth, group-delay, linearity, common-source, source degeneration.

I. INTRODUCTION

For the design of a transimpedance amplifier, the objective was to meet the predetermined specification (Table 1) using 0.13µm CMOS technology. These specifications should be met with a temperature variation of -40C to 125C and a 10% fluctuation in the supply voltage of 1.5V. Also, the bias current has to be derived from a single reference current-source of 50µA and V_{GS}, V_{GD} and V_{DS} of all 0.13µm MOSFETs have to be less than 1.2V.

Specification	Target	Final Design
Transimpedance Gain	> 3kΩ	3.49kΩ
Supply voltage	1.5V	1.5V
Power consumption	< 30mW	1.815mW
3-dB Bandwidth	2.8GHz	2.958GHz
Group delay variation	< 40ps	26.85ps
Maximum input current for linear operation	800µA	167µA
Reference Current	50µA	50µA

Table 1: Transimpedance amplifier specifications

In order to achieve the specified requirements, the design was constructed in two stages. The first stage is in shunt-shunt feedback configuration to maximize the bandwidth up to the 3 GHz cascaded to a common-source with source degeneration configuration as second stage, to pull the gain up to 3kΩ without deteriorating the overall bandwidth.

After the transimpedance amplifier was optimized for a specific gain, bandwidth and group-delay variation, it was tested for all voltage and temperature fluctuations, and maximum input current for linear operation was determined.

II. CIRCUIT DESIGN

Before deciding the upon the two-stage implementation, several other designs were tested, such as the first stage in common gate configuration with a common source feedback. These implementations were fairly close to the gain requirements but the bandwidth specification was not met. This method would have also introduced a possible chance of instability due to the presence of three poles in a feedback circuit. The two-stage implementation was finally chosen as it is stable with two poles in the feedback configuration and also meets the gain-bandwidth requirement.

As shown in figure 1, the first stage is in a shunt-shunt feedback configuration [1][2] with transistor M0 in a common source configuration, biased through a feedback resistor R_f. The input is a small-signal current source with a capacitive loading of 300fF. The DC current across transistor M0 is maintained through a current mirror acting as an active load for the first stage. Since there is no DC current passing through R_f, M0 is biased to its own drain voltage keeping it in saturation. The output of the first stage is fed to the second stage, which is a biased in a common source (with source degeneration) configuration to pull the gain up to 3kΩ without further deteriorating the bandwidth achieved in the first stage.

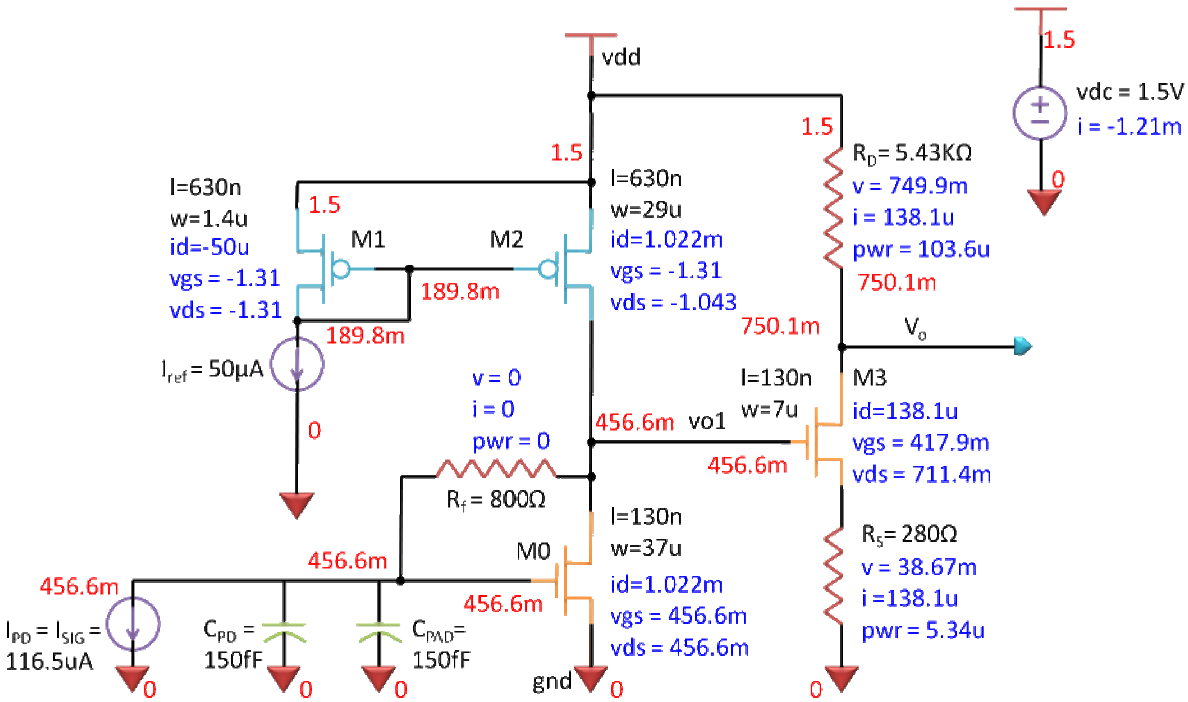

Figure 1: Transimpedance amplifier schematic with the a shunt-shunt feedback cascaded to a common source with source degeneration

To achieve the required specification, the first stage was aggressively optimized for higher bandwidth. The open loop gain A_0 obtained by removing the feedback circuit along with its loading at input and output, can be expressed as

$$A_0 = \frac{vo1}{i_{sig}} = -\frac{g_{m_0} \times {R_f}^2}{1 + s(C_{PD} + C_{PAD})R_f} \qquad - (1)$$

with two poles f1 and f2 given by

$$\mathrm{f1} = \frac{1}{2\pi R_f C_{in}}$$

$$\mathrm{f2} = \frac{1}{2\pi R_f C_{out}} \qquad - (2)$$

where,

$$C_{in} = C_{PD} + C_{PAD} + C_{GS_0} + C_{SB_0} + (1 + g_m R_f)C_{GD_0}$$

$$C_{out} = C_{DB_0} + C_{GD_0} + C_{DB_2} + C_{GD_2}$$

The resistive feedback produces a beta-factor of $-\frac{1}{R_f}$, resulting into a closed loop gain A_f expressed as,

$$A_f = -\frac{g_m \times {R_f}^2}{1 + \frac{s}{\left\{\frac{1 + g_m R_f}{(C_{PD} + C_{PAD})R_f}\right\}}} \qquad - (3)$$

With f1 being the dominating pole responsible for the bandwidth of the first stage, the 3dB frequency of the first stage can be simplified as,

$$\mathrm{f}_{3\mathrm{dB}} = \frac{\frac{1}{R_f} + g_m}{C_{in}} \qquad - (4)$$

Equation 4 elucidates three important facts about effect of R_f and g_m in increasing the bandwidth: The first is that by reducing R_f, we can have an inverse increase in bandwidth, but a quadratic decrease in gain. The second is that by increasing the width of transistor M0, the g_m increases and linearly improves both the gain and bandwidth. An increase in transistor width, however, not only increases its own intrinsic capacitance, but also the Miller-amplified capacitance due to the increase gain, resulting into an increased $C_{in.}$ Therefore, the transistor width can be increased only up to an optimum value for maximum bandwidth and gain. The third and most important fact is that an increase in DC bias current also leads to increase in g_m.

An increase in DC current poses three critical issues in the transimpedance performance. First, it increases the power consumption. Second, increasing the DC current requires increasing M2's width, which in turn introduces its own capacitance that leads to a decrease in the f2 pole's position. As f2 moves closer to the increasing f1, there needs to be a minimum spacing of $2g_m R_f$ between f1 and f2 to be characterized as a Butterworth response and avoid peaking in order to have a better control over the group delay variation. The third important issue is that as DC current increases, resistance seen at the collector end of M2 decreases. Because of this, the parallel combination of R_f and ro_3 doesn't approximate to R_f (which was the basic assumption for equation 1, 2, 3 and 4), resulting in a decreased bandwidth and gain. Therefore by increasing the length of the active load with an increase in DC current, the same resistive effect as seen for smaller DC current values is observed.

Due to the constraints discussed above, the design includes a reduced R_f with increased width of M0 and increased bias current (by maintaining proper transistor-width ratio and length of the current mirror) to have a sufficient bandwidth and minimum group delay variation as per the required specification.

Finally, for the second stage, the size of M3, R_D, and R_S were chosen with the following three considerations in mind. Firstly, the DC current and width of the transistor were decided such that the pole frequency introduced by the second stage is far away from that of the first stage. Secondly, R_D and g_m of transistor M3 were set so as to have sufficient voltage amplification to pull the transimpedance gain to 3kΩ. Finally, the DC output voltage was set to 0.75V in order to operate in the linear region. While maintaining linearity without source degeneration,, the gain was found to be much higher than the required value, resulting in a lower value for the maximum input current required for linear operation. Adding R_S as a source-degeneration resistor not only controls the DC output voltage to 0.75V, but also increases the maximum input current for linear operation.

III. SIMULATION RESULTS

The transimpedance schematic was simulated under extreme temperature fluctuations from -40C to 127C with ±10% variation in operating voltage of 1.5V. The simulation results, as shown in figure 2, 3, and 4 for -40C, 27C and 127C operating temperatures respectively, and gain, bandwidth and group-delay variation values are listed in table 1.This proves the fact that the design meets the required specifications, even under extreme conditions. For the nominal VDD of 1.5V and a temperature of 27C, the transimpedance gain obtained was 3.49kΩ, with a bandwidth of 2.958GHz and a minimum group-delay variation of 26.85ps. Due to the noise sensitivity of TIA at higher frequencies, the bandwidth was deliberately kept in the vicinity of the minimum specification which is 2.8GHz. With the given specification, the worst case scenario for the bandwidth was observed when VDD was 1.35V and temperature was set to 127C. Here the bandwidth was found to be 2.818GHz, whereas, the transimpedance-gain was at its lowest at 3.286kΩ when VDD was 1.5V at a temperature of 127C.

VDD (V)	**Temp (C)**	**Gain (kΩ)**	**Bandwidth (GHz)**	**Group Delay Variation (ps)**
1.35V	-40	3.581	2.991	24.89
	27	3.417	2.918	28.03
	127	3.211	2.818	32.82
1.5V	-40	3.654	3.035	24.3
	27	3.49	2.958	26.85
	127	3.286	2.866	30.51
1.65V	-40	3.718	3.061	23.94
	27	3.552	2.986	26.4
	127	3.348	2.89	29.62

Table 2: Gain, Bandwidth and Group-Delay variation for temperature and voltage fluctuation

The DC operating point of the transimpedance circuit as shown in figure 1 indicates that a total current of 1.21mA was drawn from the 1.5V DC source, resulting in a power consumption of 1.815mW which is considerably less than the maximum power consumption-limit of 30mW.

The only specification that was not achieved was maximum input current of 800µA for linear operation. With the desired transimpedance gain of 3kΩ and a small-signal input current of 800µA, the output voltage could swing with an AC magnitude of 2.4V. This is impossible considering the VDD at 1.5V and the output voltage biased at 0.75V for linear operation. The given requirement is not feasible with the given VDD restrictions. However, the current design of transimpedance gain of 3.49kΩ, and with the output voltage biased at 0.75V, the expected maximum input current for linear operation is 215µA. With the maximum input current defined as the allowable current leading to a 1dB decrease from the nominal transimpedance gain, figure 5 shows that with the input current level at 215µA, the gain obtained was 2.728kΩ, which is lesser than 3.11kΩ i.e. a 1dB decrease from the nominal gain of 3.49kΩ. From the Spectre simulation, figure 6 indicates that with a maximum input current of 167µA, the gain reaches to a value of 3.110kΩ. However, a slight increase to 168µA produces a gain of 3.102kΩ (less than a 1dB decrease) as shown in figure 7.

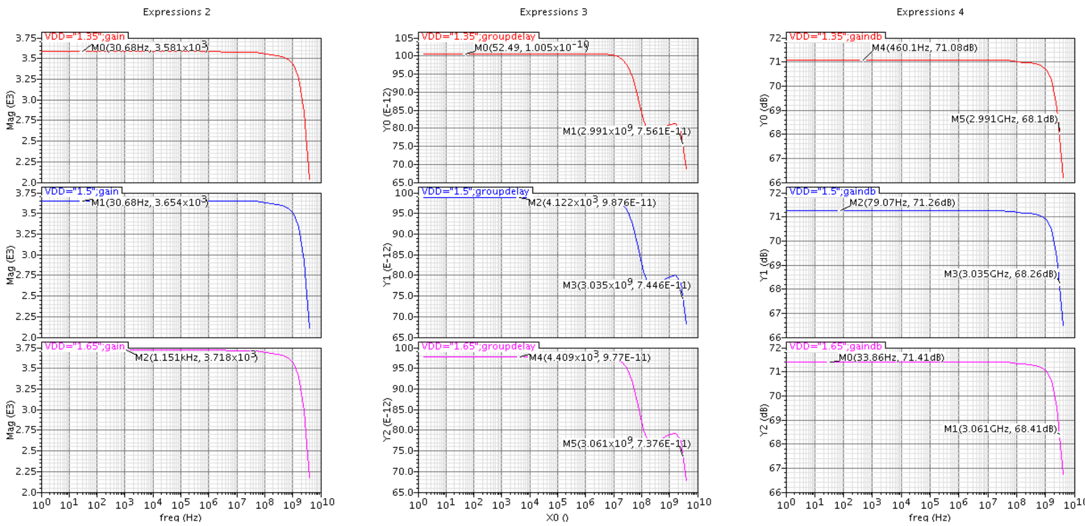

Figure 2: Gain, Group Delay and Bandwidth response for VDD = 1.5V±10% at temperature -40C

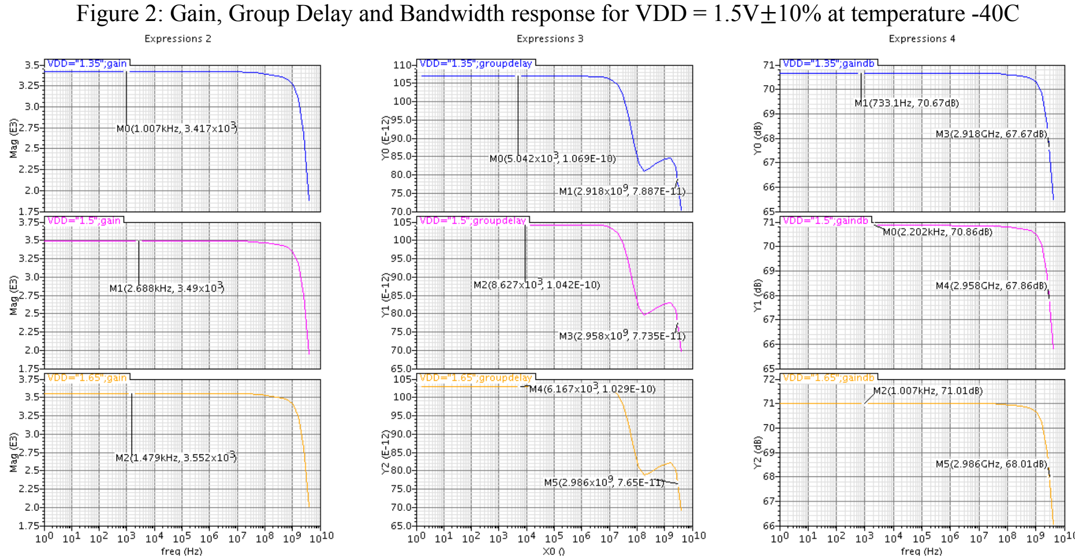

Figure 3: Gain, Group Delay and Bandwidth response for VDD = 1.5V±10% at temperature 27C

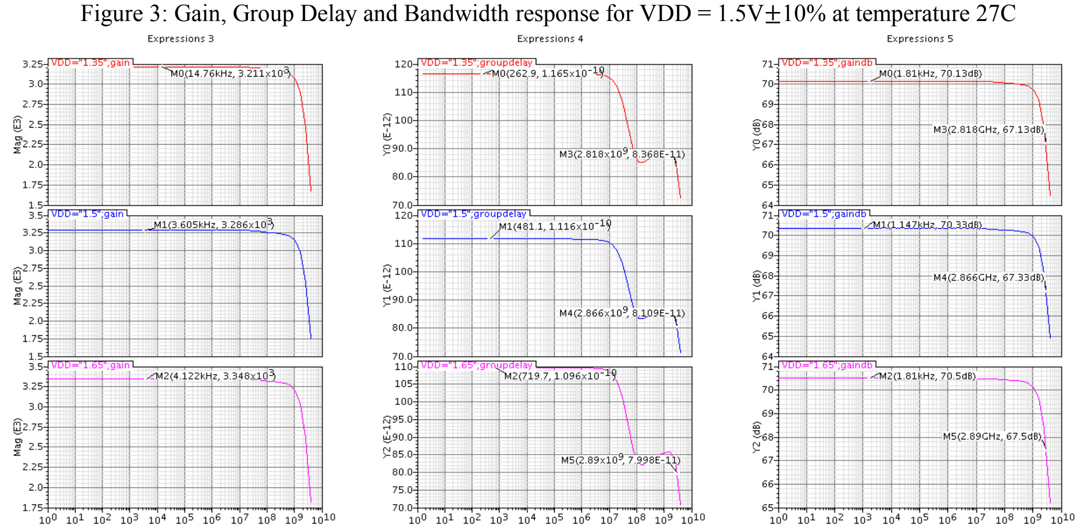

Figure 4: Gain, Group Delay and Bandwidth response for VDD = 1.5V±10% at temperature 127C

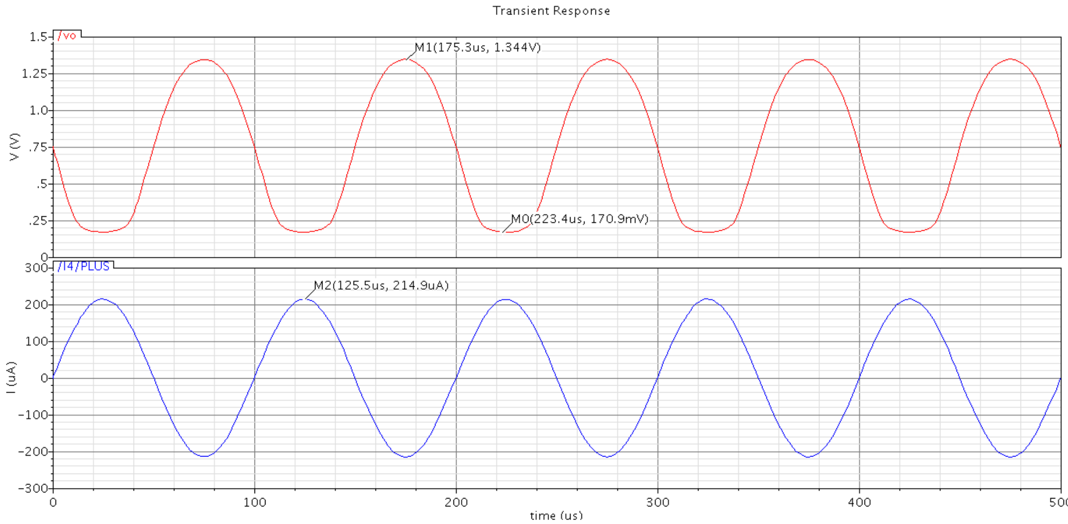

Figure 5: Transient simulation with an input current level of 215μA

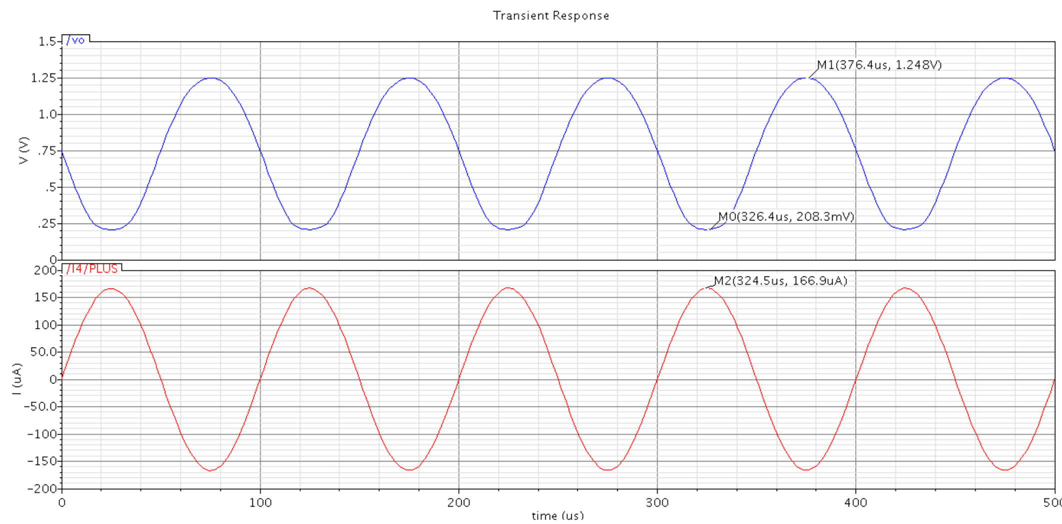

Figure 6: Transient simulation with an input current level of 167μA

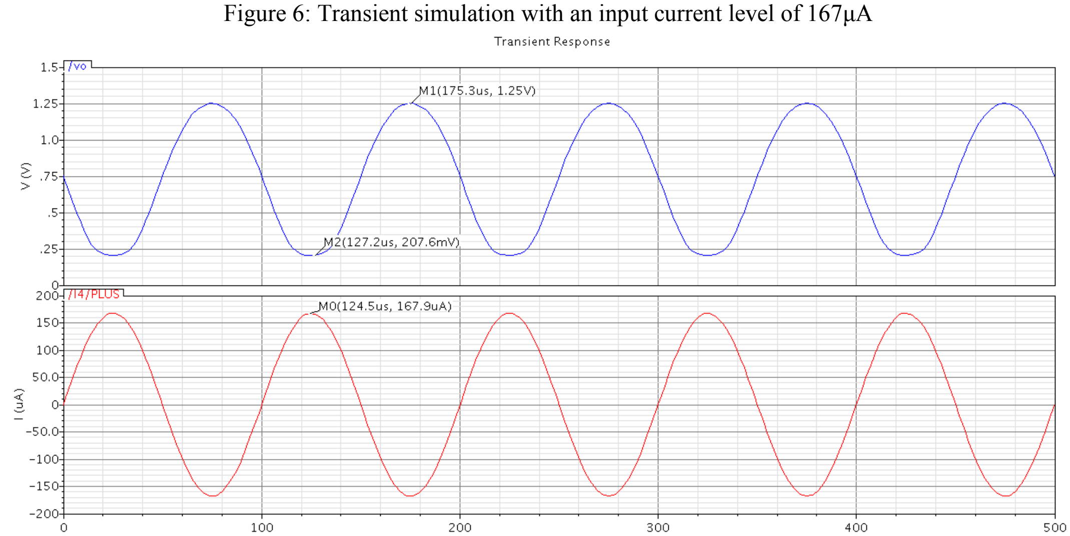

Figure 7: Transient simulation with an input current level of 168μA

IV. CONCLUSION

The design and implementation of a MOS based transimpedance amplifier has been detailed. The shunt-shunt feedback configuration of the first stage contributed greatly in achieving higher bandwidth and the second stage helped increasing the gain up to the required specification. The active load plays an important role in affecting the poles of the amplifier circuit. Therefore, it requires a careful sizing for both length and width in order to have a peaking-free gain response with minimum group-delay variation as per the requirement. Also, adding a source degeneration resistor not only helped in lowering the gain to the required value but also improved the linearity. Furthermore, the specification regarding maximum input current for linear operation to be 800μA is found to be infeasible with given VDD and gain requirements. Finally, the functionality of the transimpedance amplifier with respect to changes in the operational voltage and temperature is illustrated.

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