

ABHINANDAN MAJUMDAR

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RESEARCH INTEREST

Digital VLSI, Embedded Systems Design, Computer Architecture

EDUCATION

Columbia University, Fu Foundation SEAS, New York, NY

M.S., Computer Engineering; December 2008; GPA: 3.9/4.0

National Institute of Technology Karnataka, Surathkal, India

B.E., Computer Engineering; June 2006; Aggregate: 2577/3300

Central Board of Secondary Education, DAV Public School, Bilaspur, India

12th Board Exam; June 2002; Aggregate: 90.4%

RESEARCH EXPERIENCE

Universal Learning Machine, Feb 2009 – Present

Advisor: Dr. Srihari Cadambi, NEC Laboratories, Princeton, NJ

Currently working on the design and implementation of Universal Machine Learning architecture to run computationally-intensive algorithms on a Xilinx FPGA board.

16 Core Network On Chip Design, Feb 2008 – Present

Advisor: Prof. Kenneth Shepard, Columbia University, New York, NY

Designed the I/O pad-frame for the 16 core Network On Chip, and reduced the capacitance of Analog pad to decrease the attenuation of low-swing differential clock signal. Working towards generating a DRC/LVS clean layout image of the NoC chip.

Vulnerability of On-chip Interconnection Networks to Soft Errors, Feb 2008 – May 2008

Advisors: Prof. Simha Sethumadhavan and Prof. Luca Carloni, Columbia University, New York, NY

Estimated the soft-error trend for an RTL model of a wormhole router and observed a linear increase in soft-error rate with device-size scaling from 90nm to 22nm CMOS technology

FPGA Implementation of Integer Linear Programming Accelerator, June 2005 – July 2005

Advisor: Prof. M. Balakrishnan, Indian Institute of Technology, Delhi, India

Designed and implemented an RTL based design of Simplex Algorithm on FPGA and obtained a speed-up over software implementation.

PROJECT EXPERIENCE

Trans-impedance Amplifier Design, Fall 2008

Course: Analog Electronic Circuits, Instructor: Prof. Timothy Dickson, Columbia University, New York, NY

Designed a trans-impedance amplifier, at schematic level, with an input loading of 300fF, a trans-impedance gain of 3K Ω and a bandwidth of 2.8GHz using 130nm TSMC technology.

FPGA Implementation of Integer Linear Programming Accelerator, Spring 2008

Course: Embedded System Design, Instructor: Prof. Stephen Edwards, Columbia University, New York, NY

Designed and implemented a high speed AES Decryptor to decrypt the encrypted image-sequences stored in a SD card and display it over a VGA monitor as a slide show.

4 Kilobyte SRAM Array, Fall 2007

Course: VLSI Circuits, Instructor: Prof. Azeez Bhavnagarwala, Columbia University, New York, NY

Implemented a DRC/LVS clean design of high speed domino logic implementation of Address-Decoder, and 64x64 SRAM array with pre-charge, read and write circuitry using IBM 90nm technology.

Channel Equalization, Fall 2007

Course: Digital Signal Processing, Instructor: Prof. Dan Ellis, Columbia University, New York, NY

Inferred the unknown filter effects induced on a sound signal, and corrected the spectrum by inverting the filter effects.

Hardware and Software Optimization of Matrix Multiplication, Fall 2007

Course: Computer Architecture, Instructor: Prof. Luca Carloni, Columbia University, New York, NY

Optimized the software implementation of Matrix Multiplication by dynamic algorithm and multithreading, and optimized the hardware for a specific cost requirement using SESC simulator.

Formal Verification of GCD Unit, Fall 2007

Course: Formal Verification, Instructor: Prof. Michael Theobald, Columbia University, New York, NY

Formally verified an RTL implementation of GCD unit using VIS for both the basic and failure cases.

Reconfigurable Computing for DSP Application, Semester 7th and 8th

Course: Project, Advisor: Prof. Ramesh Kini, NITK Surathkal, India

Analyzed and implemented the MP3 algorithm (up to quantization phase) on FPGA.

C compiler for C language, Semester 6th

Course: Compilers, Instructor: Prof. Santhi Thilagam, NITK Surathkal, India

Designed a C compiler from lexical analysis to intermediate-code-generation stage using Flex and Yacc tool

On-line Credit Card Transaction System, Semester 5th

Course: Database, Instructor: Prof. Saumya Heghde, NITK Surathkal, India

Designed a relational database-model of the credit-card transaction system using Oracle, retrieved the specific entries through SQL queries and designed the front-end user-interface using VB.

PDP-11 Assembler and Simulator, Semester 4th

Course: Systems Programming, Instructor: Prof. Nagesh, NITK Surathkal, India

Implemented a PDP11 Assembler from lexical analysis to machine-code generation using C, and implemented an artificial simulation environment to execute the generated machine-level code.

**WORK
EXPERIENCE**

Intel Technology, Bangalore, India, July 2006 – July 2007

Developed configuration and memory test tool, and enhanced Readyboost and Readydrive features for Intel Turbo Memory Module (ROBSON).

PUBLICATION

Abhinandan Majumdar, “FPGA Implementation of Integer Linear Programming Accelerator”, International Conference on Systemics, Cybernetics and Informatics (ICSCI), SC-2.2, January 2006.

**TEACHING
EXPERIENCE**

MS Teaching Assistant, Fall 2008

Assisted Prof. Steven Nowick in his graduate-level course “Advanced Logic Design”. Helped create curriculum, led weekly office hours, maintained the course website, composed assignment solutions and graded all the written work.

MS Teaching Assistant, Fall 2008

Assisted Prof. Dan Rubenstein in his undergraduate-level course “Fundamentals of Computer Systems”. Led weekly office hours with the students, composed assignment solutions and graded the midterm and final exams.

MS Teaching Assistant, Spring 2008

Assisted Prof. Pranav Ashar in his graduate-level course “Advanced Logic Design”. Helped create curriculum, led weekly office hours with the students, composed assignment solutions and graded the project and final exams.

MS Teaching Assistant, Spring 2008

Assisted Prof. Simha Sethumadhavan in his undergraduate-level course “Fundamentals of Computer Systems”. Led weekly office hours, composed assignment solutions and graded the midterm and final exams.

Grader, Fall 2008

Assisted Prof. Dan Rubenstein in his undergraduate-level course “Fundamentals of Computer Systems” in grading all the written submissions.

**FELLOWSHIP
AND AWARDS**

- Full MS Teaching Assistant Fellowship of \$21,696 with \$3000 stipend per term for Spring and Fall 2008, Computer Science Department, Columbia University, 2008.
- Outreach Grant Scholarship of \$2,500, International House, New York, 2007-2008.
- Spontaneous Recognition Award, Intel Technology, 2007.
- Best Paper Award, ICSCI, 2006.
- Best Student Award for first position in 12th Board, DAV Public School, 2002.
- Certificate of Honor for second position in state engineering exam, 2002.
- Certificate of Merit, National Mathematics Olympiad, 1999.

**COURSES
TAKEN**

Master of Science, Columbia University, NY
VLSI Circuits, Analog Electronic Circuits, Embedded System Design, Topics in Electronic Circuits, Distributed Embedded System, Computer Architecture, Digital Signal Processing, Formal Verification.

Bachelor of Engineering, NITK Surathkal, India
Digital Systems, Logic Design, Computer Organization, Computer Architecture, Microprocessors, Operating Systems, Algorithms, Computer Networks, Graphics, Database Systems, Compilers, Data Structures, Programming Languages, Software Engineering, Operations Research, Object Oriented Systems, Data Communications, Theory of Computation, Systems Programming, Principles of Programming Languages.

**TECHNICAL
SKILLS**

Hardware
Cadence: Virtuoso Schematic, Virtuoso Layout, SoC Encounter, HSPICE, Spectre, Analog environment, UltraSim
Mentor: Calibre DRC/LVS/xRC, ModelSim.
FPGA tools: Altera's Quartus, Xilinx ISE
VHSIC: VHDL, Verilog.

Software
C, Java, Win32, TASM, Shell, FLEX, YACC, MATLAB, VB, Oracle, SQL

**PERSONAL
DETAILS**

Official Name on US documents: Majumdar Abhinandan
Citizenship: India
Visa Status: F-1