

## ABHINANDAN MAJUMDAR

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### EDUCATION

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<b>Columbia University, School of Engineering and Applied Sciences, New York, NY</b> Master of Science in Computer Engineering	<b>Expected in Dec. 2008</b> <b>CGPA: 3.9/4.0</b>
<b>National Institute of Technology Karnataka, Surathkal, INDIA</b> Bachelor of Engineering in Computer Engineering	<b>Completed in June 2006</b> <b>Aggregate: 81%</b>

### RELEVANT COURSE WORK

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<b>Graduate</b>	Digital VLSI, Analog Circuits, Embedded System Design, Computer Architecture, Digital Signal Processing
<b>Undergraduate</b>	Algorithms, Operating Systems, Database, Compilers, Microprocessors, Logic Design, Computer Organization, Data Structures, Programming Languages

### WORK EXPERIENCE

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<b>NEC Research Lab, Columbia University, New York, NY</b> <i>Research Assistant</i> , Universal Learning Machine	<b>Feb 2009 – Present</b>
<ul style="list-style-type: none"><li>Currently working on designing and prototyping a Universal Learning Machine on a Xilinx FPGA.</li></ul>	
<b>Columbia Integrated Systems Lab, Columbia University, New York, NY</b> <i>Research Intern/Assistant</i> , 16 Core Network On Chip Design	<b>Feb 2008 – Present</b>
<ul style="list-style-type: none"><li>Currently working on place and route of the entire network-on-chip.</li><li>Implemented a LVS clean I/O pad-ring reduced the capacitance of ANALOG pad for the entire 16 core Network on Chip.</li></ul>	
<b>Intel Technology, Bangalore, India</b> <i>Software Engineer</i> , Intel® Turbo Memory Module (ROBSON)	<b>July 2006 – July 2007</b>
<ul style="list-style-type: none"><li>Developed configuration and memory test tool for ROBSON device.</li><li>Enhanced Readyboost and Readydrive features for ROBSON Driver.</li></ul>	
<b>Indian Institute of Technology, Delhi, India</b> <i>Summer Intern</i> , FPGA Implementation of Integer Linear Programming Accelerator	<b>June 2005 – July 2005</b>
<ul style="list-style-type: none"><li>Designed and implemented Simplex Algorithm on Xilinx Virtex II FPGA and obtained a speed-up over C implementation.</li></ul>	

### PROJECT EXPERIENCE

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<b>Design of a MOS-based Transimpedance Amplifier for a Transceiver-level receiver application</b>	<b>Fall 2008</b>
<ul style="list-style-type: none"><li>Designed a two stage amplifier; shunt-shunt feedback cascaded to a common source degeneration configuration.</li><li>Optimized the design to achieve a transimpedance gain of 3.49kΩ and a bandwidth of 2.96GHz.</li></ul>	
<b>Vulnerability of On-chip Interconnection Networks to Soft Errors</b>	<b>Spring 2008</b>
<ul style="list-style-type: none"><li>Designed a synthesizable RTL design of Wormhole Router and validated the design for 3x3 mesh network.</li><li>Computed the Soft-Error Rate for the router and observed a linear increase in SER with technology scaling.</li></ul>	
<b>FPGA Implementation of Integer Linear Programming Accelerator</b>	<b>Spring 2008</b>
<ul style="list-style-type: none"><li>Designed and Implemented the AES Decryption Algorithm over Altera Cyclone II FPGA.</li><li>Designed the SRAM implementation to store the decoded image and display the image on the VGA monitor.</li></ul>	
<b>4 Kilobyte SRAM Array</b>	<b>Fall 2007</b>
<ul style="list-style-type: none"><li>Implemented a DRC/LVS clean design of high speed domino logic implementation of Address-Decoder</li><li>Implemented a LVS clean design of 64x64 SRAM array with pre-charge, read and write circuitry.</li></ul>	

### TECHNICAL SKILLS

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<b>Hardware</b>	Virtuoso, HSPICE, Spectre, Analog environment, Ultrasim, SoC Encounter, Calibre DRC/LVS/xRC, VHDL, Verilog
<b>Software</b>	C, WIN32, SHELL, FLEX, YACC, MATLAB, SKILL

### ACHIEVEMENTS

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- MS Teaching Assistant Fellowship for year 2008 from Computer Science Department, Columbia University.
- SPONTANEOUS RECOGNITION AWARD from Intel Technology Bangalore.
- Paper titled "FPGA IMPLEMENTATION OF INTEGER LINEAR PROGRAMMING ACCELERATOR", received "Best Paper Submission" at International Conference of Systemics Cybernetics and Informatics -2006.